AMENDMENT(S) TO THE SPECIFICATION:

Kindly amend paragraph 7 on page 2 as follows:

In one such arrangement, the MAC processing functions are divided between a "Lower MAC" that implements in hardware such ~~aspects~~ aspects as interfacing to the physical radio (the PHY) 101, encryption, and the actual receiving and sending of MAC packets. The Lower MAC may be implemented using a processor and includes a local memory. The "Higher MAC" functions, i.e., the remaining MAC functions are implemented in software running on a host processor. The Lower MAC is coupled to the host processor via a bus subsystem.

Kindly amend paragraph 8 on page 2 as follows:

When to-be-transmitted packets are ready, the host passes information to the Lower MAC on such packets. The information, for example, may include information on where the payload for the MAC packets resides in the host memory. This information is stored locally on the Lower MAC. When the Lower MAC ~~is sets~~ is set up to transmit the to-be-transmitted MAC packets, the Lower MAC ~~is sets~~ sets up a DMA transfer of the required data. The data is then passed to the Lower MAC processor via DMA from the host.

Kindly amend paragraph 31 on page 6 as follows:

FIG. 2 shows a wireless station for implementing an access point (AP) coupled to a network switch 229 via a network link 228, typically a wired network connection such as an Ethernet connection. The MAC processing functions of the station 200 are divided between a "Lower MAC" 203 that implements such ~~aspects~~ aspects as interfacing to the physical radio (the PHY) 101 using a PHY interface 217, encryption/decryption using a cryptography engine 221, and the actual receiving and sending of MAC packets in a MAC packet and DMA engine 223. The "Higher MAC" functions, i.e., the remaining MAC functions are implemented in software running on a host processor 211. The Lower MAC 203 is coupled to a host processor 211 via a bus subsystem 209. Coupled to the host bus are also a host DMA controller 207 and a host memory interface 213 to which host memory 215 is connected.

Kindly amend paragraph 36 on page 7 as follows:

Consider as an example the host processor receiving packets ~~for~~ via the network 228 that are for wireless transmission. When the host processor has new packets ready for transmission, it informs the Lower MAC 203 by providing the Lower MAC with information sufficient to set-up the transmission. This information includes the MAC headers for the packets for transmission, the location of any data required for building a MAC packet, and information on how to construct the MAC packet from the data. In one embodiment, the information provided to the Lower MAC 203 by the host includes a set of data structures—called "buffer descriptors" herein—that include where the data for the MAC packets is located, e.g., in the host memory 215.

Kindly amend paragraph 47 on page 9 as follows:

When receiving data, the process is basically reversed. In an information exchange, the lower MAC receives from the host processor 211 the addresses where packets that are received in may be stored. In particular, the Lower MAC 203 maintains a set of receive buffer descriptor chains for receiving packets. A receive buffer descriptor chain ~~include~~ includes receive buffer descriptors that indicate where in the host memory 215 the data for received packets may be stored. When data is received via the PHY interface 217, the packet/DMA engine 223 sets us the data transfer, including possibly passing through the cryptography engine 221 for decryption. The DMA engine in the packet/DMA engine sets up the required scatter/gather list for DMA transfers and communicates this information to the Host DMA controller. The host DMA controller has access to a memory map that indicates where in memory, e.g., on the host memory 215, the data is to be written, and sets up the each DMA transfer to host memory.

Kindly amend paragraph 56 on page 11 as follows:

One aspect of the invention is that at least some of the data of MAC packets that are for wireless transmission are streamed during transmit time across the network link 328 from the switch memory to the lower MAC 303 for transmission by the PHY 101 such that data does not need to be queued in the host memory. Another aspect is that data received by the PHY 101 may be directly streamed to the switch during ~~transmit~~ receive time across the network link 328 such that received data need not be queued in the host memory. The inventors recognize that wired networks are becoming sufficiently fast to provide such streaming. In the preferred embodiment, the network 328 is a Gigabit Ethernet network. Of course, that means any Ethernet network link at least as fast as an Ethernet network link may be substituted and is within the scope of the term "Gigabit Ethernet" for purposes the invention.

Kindly amend paragraph 99 on page 20 as follows:

Note that the inventors found that for the presently available ~~the~~ IEEE 802.11 standards, an Ethernet that is at least as fast as a Gigabit Ethernet provides the required latency time. The invention, however, is not restricted to using an Ethernet for the link between the station and the network device, and also for using a Gigabit Ethernet or faster link. For example, a wireless network protocol may ~~in~~ be used that is slow enough such that a 100MB Ethernet link may be used. Also, faster wireless protocols may be introduced that require a link of at least a 10GB Ethernet. All these are meant to be included in the scope of the invention.

Kindly delete paragraph 100 on page 20:

~~ose in the aeabove embodiment The station is coupled to a network device, in one embodiment, a switch, by a network link in one embodiment, a Gigabit Ethernet or any Ethernet at least as fast as a Gigabit Ethernet. The network device includes a memory. The method is of streaming data over the network link from or to the network device memory during wirelessly transmitting or wirelessly receiving at the station.~~